# CLAIMS

1. A processor, comprising:

   a cache capable of storing data;

   a control logic capable of controlling a flow of data; and

5      at least one core coupled to the cache and the control logic, capable of generating

   a multiple of a CPU clock signal having,

        an instruction cache capable of storing data;

        an instruction fetch unit capable of fetching data;

        a plurality of integer execution units coupled to the instruction fetch unit;

10      and

        a single floating point graphics unit coupled to the plurality of integer

   execution units including circuitry capable of generating the multiple of the CPU

   clock signal.

15 2. A processor of claim 1, further comprising a delay-locked loop (DLL) circuit

   having a charge pump, the DLL circuit being capable of generating the multiple

   of the CPU clock signal.

3. A processor of claim 2, wherein the DLL circuit comprises a voltage control delay

20      line unit capable of generating multiple signals.

4. A processor of claim 2, wherein the DLL circuit further comprises a control signal capable of controlling the CPU clock signal by propagating through a plurality of inverters.

5    5. A processor of claim 4, wherein the charge pump locks the control signal to an analog value between about 0.3V and about 0.8V.

6. A processor of claim 2, wherein the DLL circuit further comprises at least one symmetric NOR and one symmetric NAND capable of combining signals.

10

7. A processor of claim 3, wherein the voltage control delay line unit further comprises a delay unit having at least two inverters capable of delaying the CPU clock signal.

15    8. A processor of claim 7, wherein signals from at least two inverters are manipulated into a control signal by a phase frequency detector and the charge pump.

9. A processor of claim 8, wherein at least two signals are manipulated by the phase frequency.

20    frequency.

10. A processor of claim 2, wherein the DLL circuit further comprises a charge pump having a Schmitt circuit, capable of increasing or decreasing voltage.

5   11. A processor of claim 2, wherein the DLL circuit further comprises at least one symmetric NOR and at least one symmetric NAND capable of combining signals.

12. A processor of claim 1, wherein the multiple of the CPU clock signal comprises a higher frequency clock having a higher frequency than the CPU clock signal.

10

13. A processor of claim 1, wherein the single floating-point graphics unit comprises a multiplier pipeline and an adder pipeline.

14. A circuit, comprising:

a floating point graphics unit having,

a voltage control delay line unit capable of generating multiple delayed

clock signals;

5          a phase frequency detector coupled to the voltage control delay line

unit capable of detecting phase differences;

a charge pump coupled to the phase frequency detector and the voltage

control delay line unit capable of increasing or decreasing voltage;

at least one symmetric NOR coupled to the voltage control delay line

10         unit capable of combining signals with identical rising edges;

at least one symmetric NAND coupled to the at least one symmetric

NOR capable of combining signals with identical falling edges; and

a buffer coupled to the at least one symmetric NAND capable of

buffering a multiple of a CPU clock signal.

15

15. A circuit of claim 14, wherein a DLL circuit comprises a delay unit capable of

delaying a signal after receiving a CPU clock signal and a control signal.

16. A circuit of claim 15, further comprising a plurality of inverters capable of

20         delaying the CPU clock signal.

17. A circuit of claim 14, wherein a control signal capable of controlling the CPU clock signal is an analog value.

18. A circuit of claim 15, wherein the multiple of the CPU clock signal is a higher
5    frequency than the CPU clock signal.

19. A method for generating a custom clock frequency comprising:

receiving a CPU clock signal;

delaying the CPU clock signal with at least two inverters;

10    generating a plurality of output signals; and

combining a plurality of signals from the plurality of output signals to generate a combined custom clock signal.

20. A method of claim 19, further comprising regulating a control signal with a first
15    signal and a last signal from the plurality of output signals.